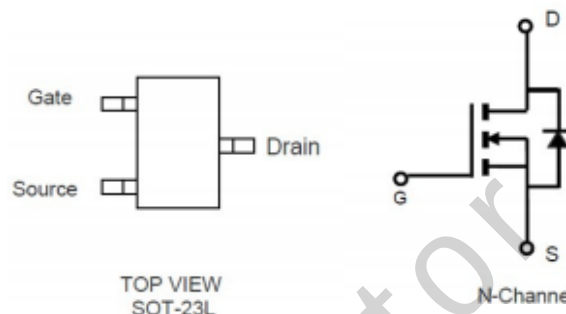


■ FEATURE

- ◆ 20V/4.5A, $R_{DS(ON)}=25m\Omega$ (typ.)@ $V_{GS}=4.5V$
- ◆ 20V/2.5A, $R_{DS(ON)}=55m\Omega$ (typ.)@ $V_{GS}=2.5V$
- ◆ 20V/2.0A, $R_{DS(ON)}=80m\Omega$ (typ.)@ $V_{GS}=1.8V$
- ◆ Super high design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and Maximum DC current capability
- ◆ Full RoHS compliance
- ◆ SOT23-3L package design



■ DESCRIPTION

The SPN3414 is the N-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

■ APPLICATIONS

- ◆ Power Management
- ◆ Portable Equipment
- ◆ DC/DC Converter
- ◆ Load Switch
- ◆ DSC
- ◆ LCD Display inverter

■ ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ C$ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V _{DSS}	Drain-Source Voltage		20	V
V _{GSS}	Gate-Source Voltage		±10	V
I _D	Continuous Drain Current (T _C =25℃)	V _{GS} =10V	4.5	A
	Continuous Drain Current (T _C =70℃)		3.0	
I _{DM}	Pulsed Drain Current		20	A
I _S	Continuous Source Current (Diode Conduction)		1.5	A
P _D	Power Dissipation	T _A =25℃	1.5	W
		T _A =70℃	0.9	
T _J	Operation Junction Temperature		150	℃
T _{STG}	Storage Temperature Range		-55~+150	℃
R _{θJA}	Thermal Resistance Junction to Ambient		90	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress rating only and functional device operation is not implied

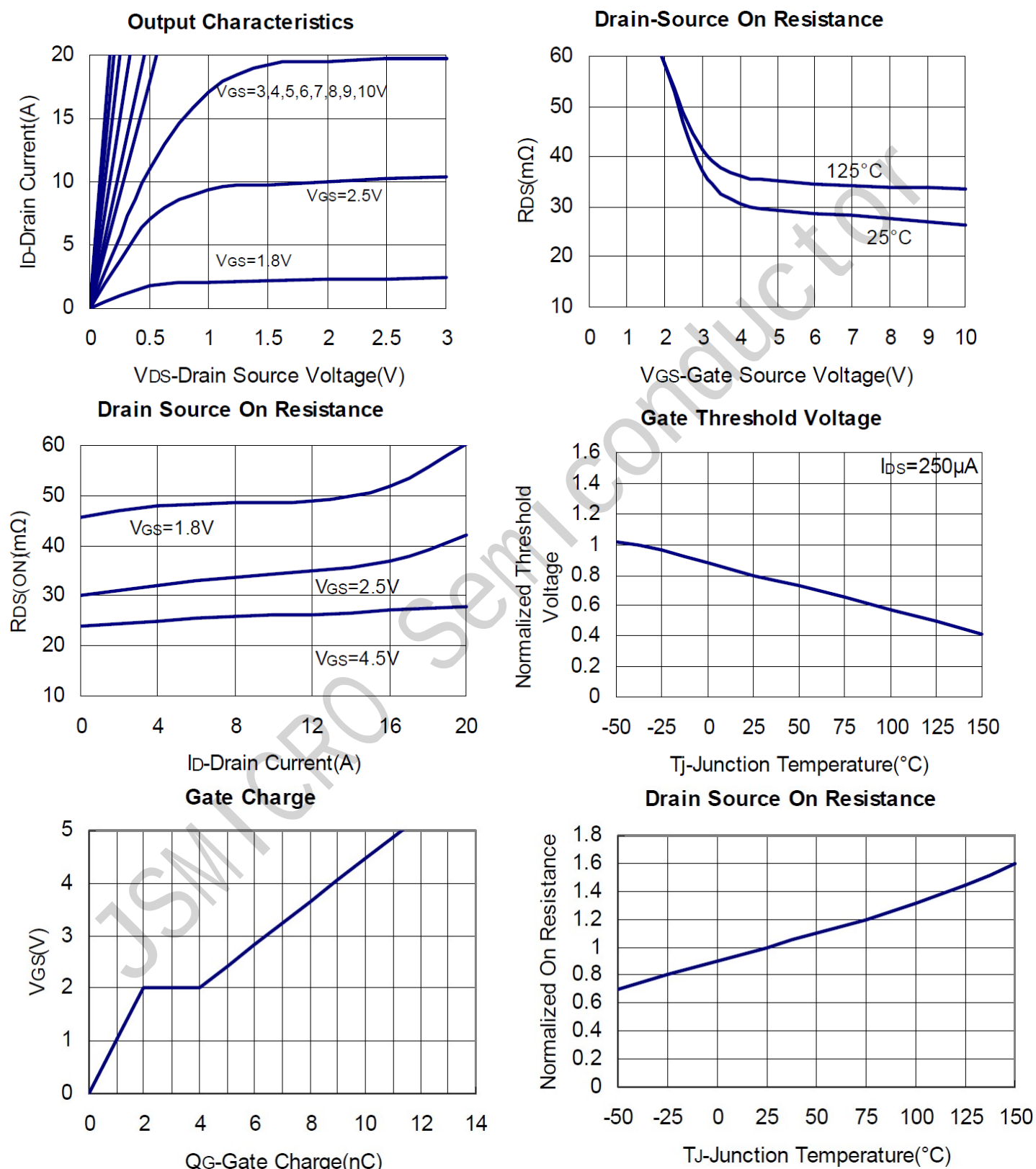
■ **ELECTRICAL CHARACTERISTICS** ($T_A=25^\circ\text{C}$ Unless otherwise noted)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	20			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250uA	0.5		1.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±12V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0			1	uA
		V _{DS} =20V, V _{GS} =0 T _J =55℃			5	
R _{DS(ON)}	Drain-Source On-Resistance	V _{GS} =4.5V, I _D =3.0A		25	45	mΩ
		V _{GS} =2.5V, I _D =2.5A		40	60	
		V _{GS} =1.8V, I _D =2.0A		65	90	
Source-Drain Diode						
V _{SD}	Diode Forward Voltage	I _S =1.7A, V _{GS} =0V		0.78	1.2	V
Dynamic Parameters						
Q _g	Total Gate Charge	V _{DS} =10V V _{GS} =4.5V I _D =5.0A		11	13	nC
Q _{gs}	Gate-Source Charge			1.45		
Q _{gd}	Gate-Drain Charge			2.3		
C _{iss}	Input Capacitance	V _{DS} =10V		578		pF
C _{oss}	Output Capacitance	V _{GS} =0V		116		
C _{rss}	Reverse Transfer Capacitance	f=1MHz		96		
T _{d(on)}	Turn-On Time	V _{DS} =10V I _D =1.0A		14.5	25	nS
T _r				42	62	
T _{d(off)}	Turn-Off Time	V _{GEN} =4.5V R _G =6Ω		46	67	
T _f				34	43	

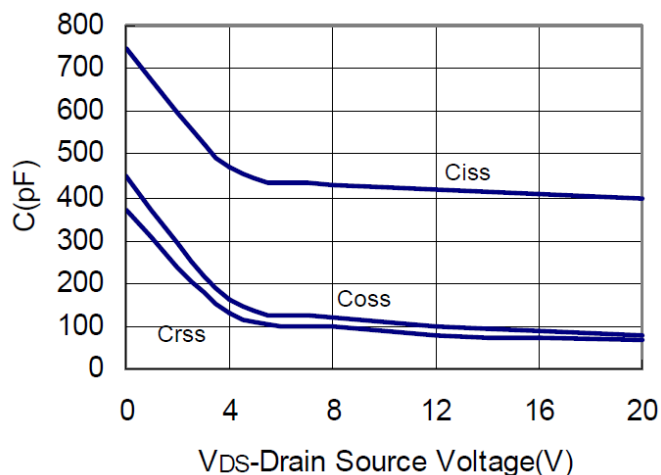
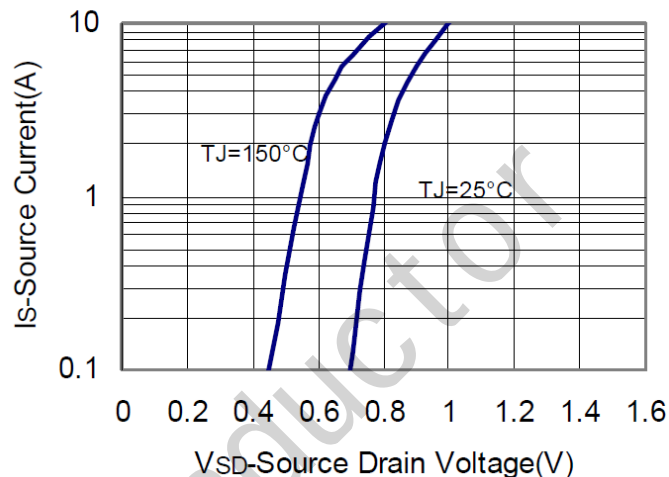
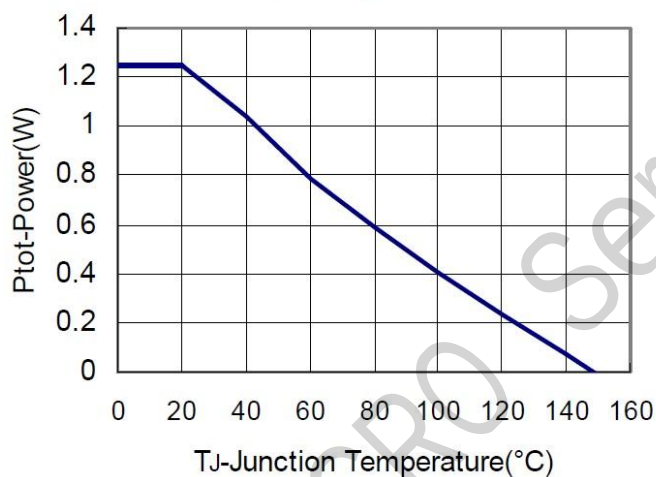
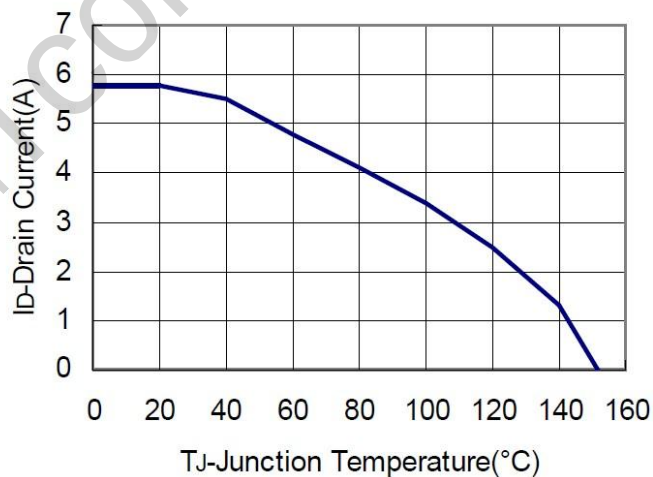
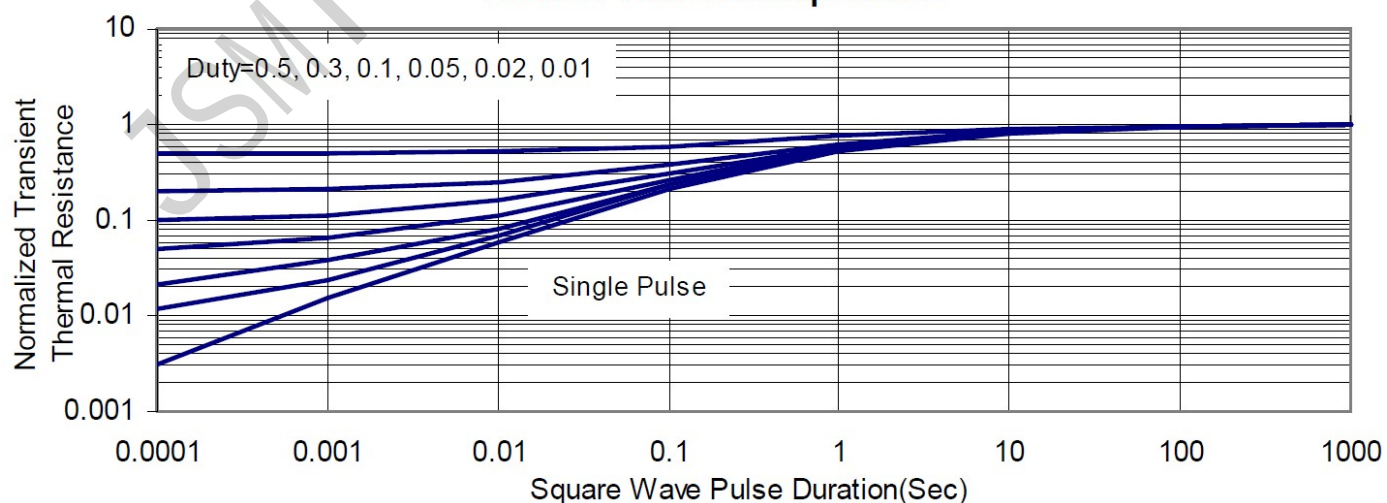
Note: 1. Pulse test: pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$

2. Static parameters are based on package level with recommended wire bonding

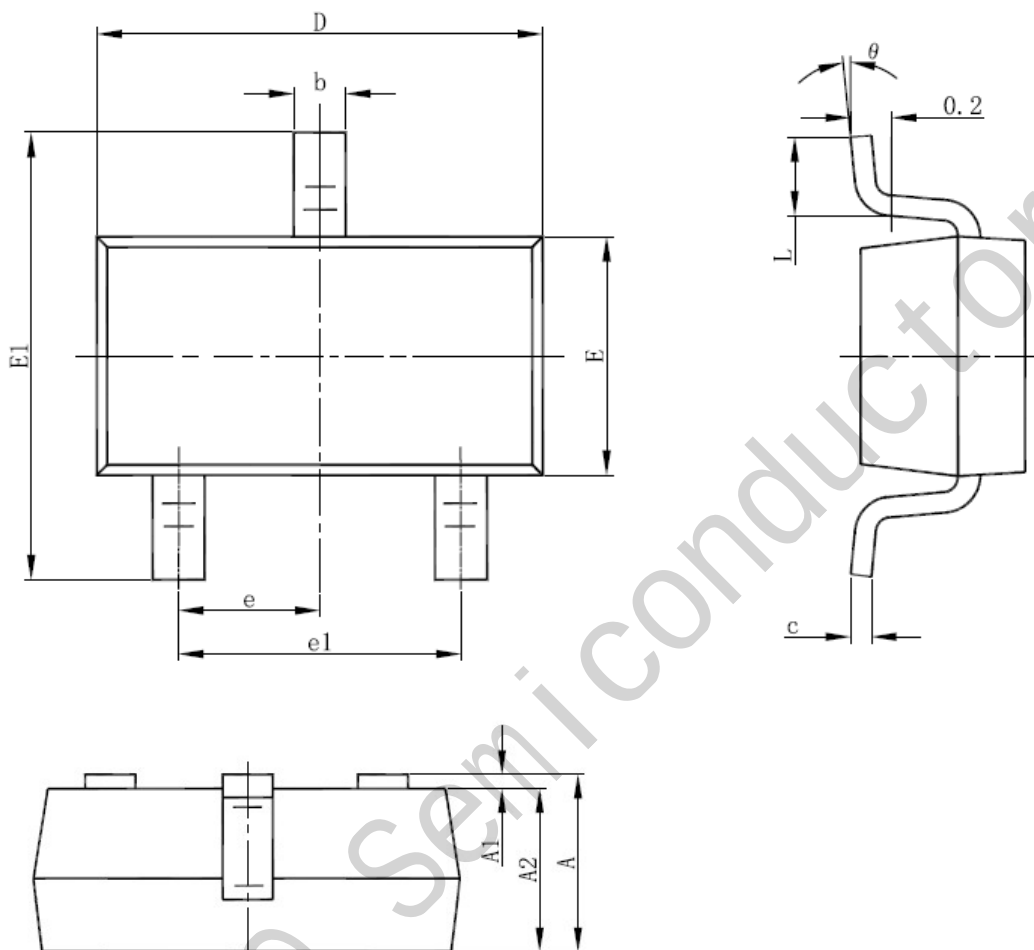
■ **TYPICAL CHARACTERISTICS** (25 °C Unless Note)



■ **TYPICAL CHARACTERISTICS** (continuous)

Capacitance

Source Drain Diode Forward

Power Dissipation

Drain Current

Thermal Transient Impedance


■ SOT23-3L PACKAGE OUTLINE DIMENSIONS



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°